Reliable, Low Cost Distributed Generator/Utility System Interconnect

NREL Quarterly Review Meeting

Oct. 23-25, 2001

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GE Corporate Research & Development

GE Power Systems Energy Consulting

Puget Sound Energy

Program Overview

2001 2002 2003 2004

Base Year

- Fundamental research through virtual test bed
- Interconnect conceptual design
- IEEE P1547 support

Optional Year I

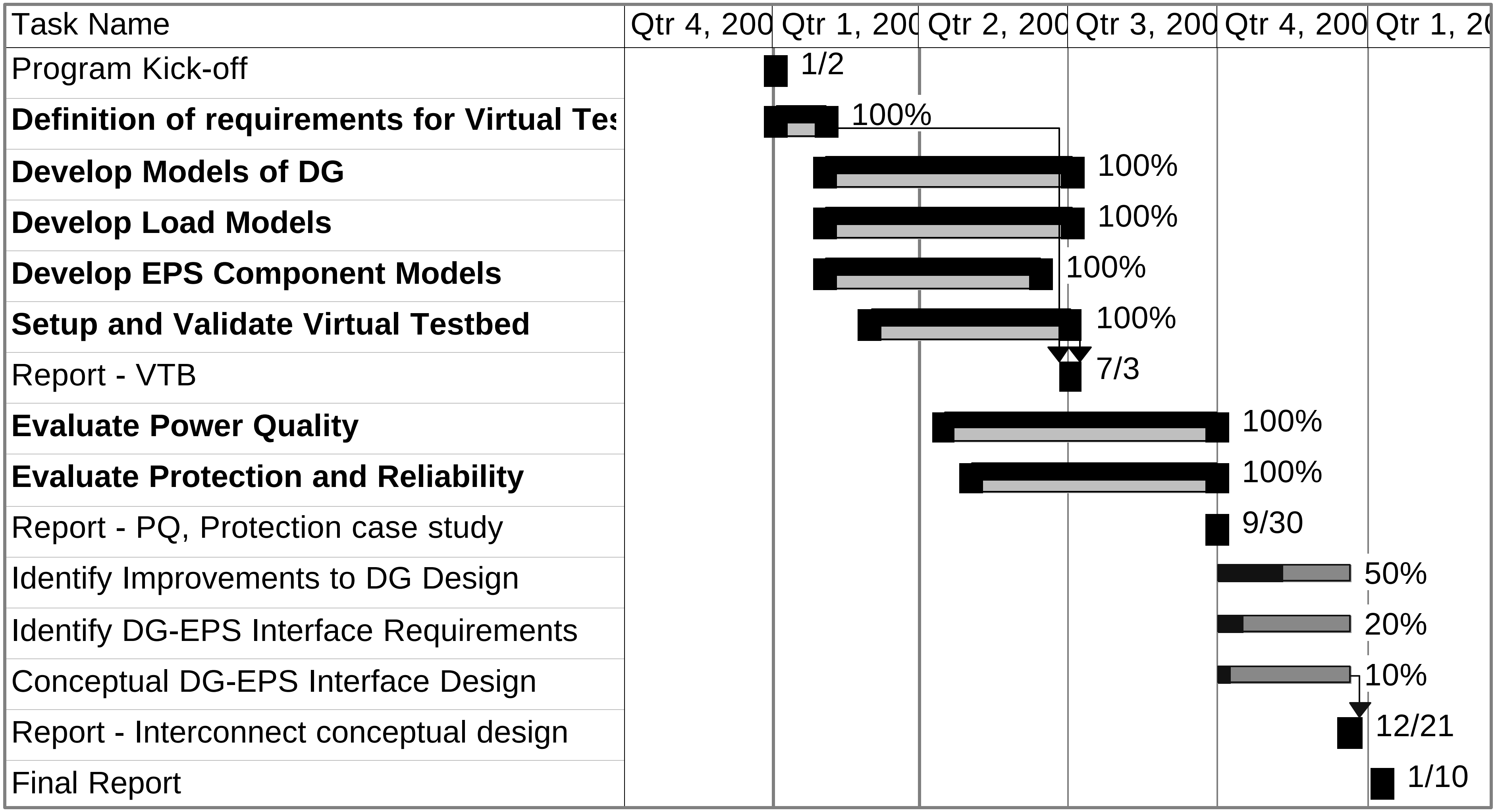
- Interconnect prototyping
- Beta test site
- Evaluate performance

Optional Year II

- Demand side management
- Cost optimization
- Beta test site

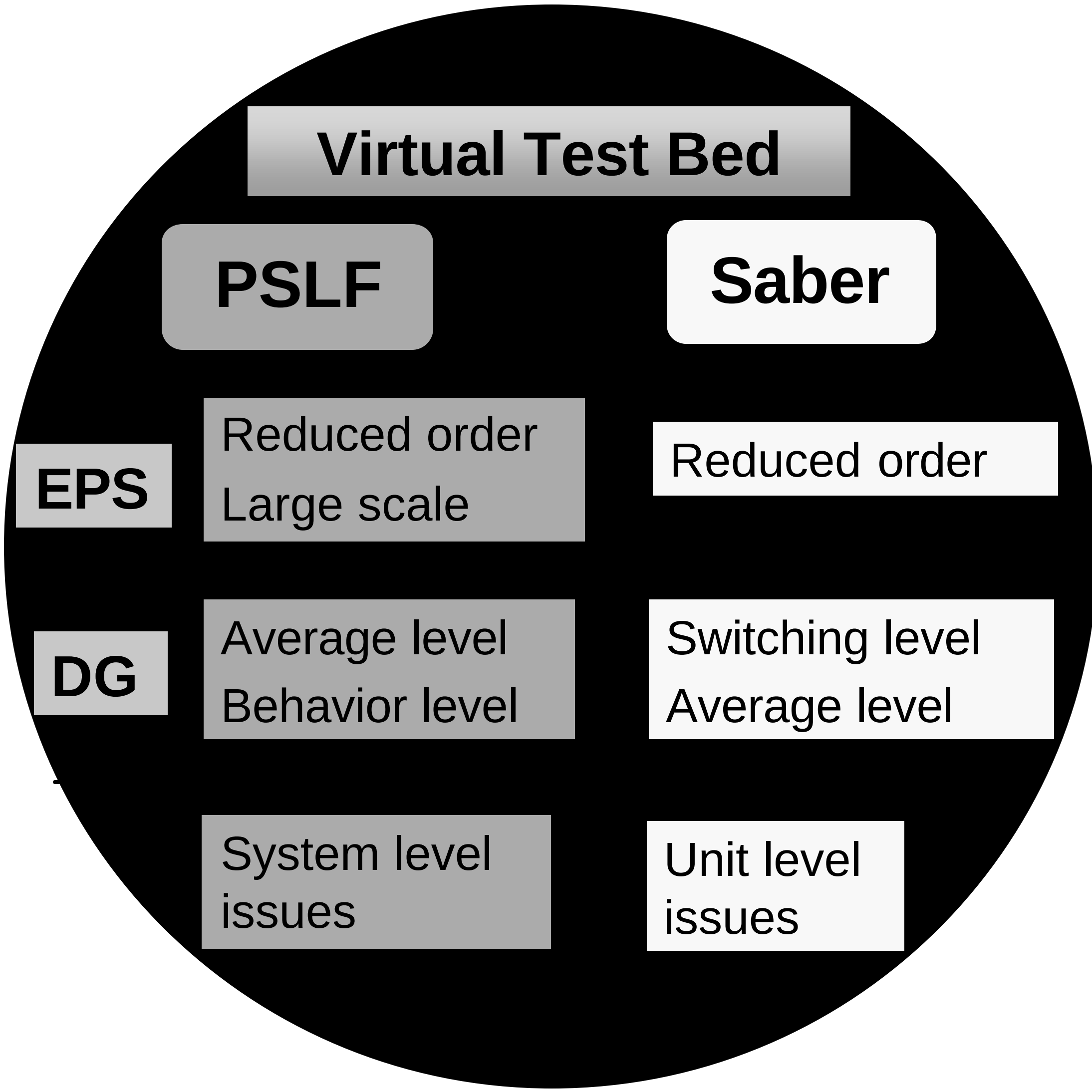
- **Outcome of Base Year**
- **Other NREL DP Programs**
- **Marketplace**

Gant Chart



Task Name
Qtr 4, 200
Qtr 1, 200
Qtr 2, 200
Qtr 3, 200
Qtr 4, 200
Qtr 1, 20
Program Kick-off
1/2
Definition of requirements for Virtual Tes
100%
Develop Models of DG
100%
Develop Load Models
100%
Develop EPS Component Models
100%
Setup and Validate Virtual Testbed
100%
Report - VTB
7/3
Evaluate Power Quality
100%
Evaluate Protection and Reliability
100%
Report - PQ, Protection case study
9/30
Identify Improvements to DG Design
50%
Identify DG-EPS Interface Requirements
20%
Conceptual DG-EPS Interface Design
10%
Report - Interconnect conceptual design
12/21
Final Report
1/10

Virtual Test Bed - Structure



Why PSLF and Saber?

- Saber - powerful system modeling tools for mixed technologies
  - Detailed transient simulation
  - Entire system modeled by differential equations

$$V = R \cdot I + L \cdot {dI}/{dt} + C \cdot \int I \cdot dt$$

  - Unlimited bandwidth
- PSLF - industry standard modeling tool for analyzing large system response
  - “Fundamental Frequency Program”
  - Power grid modeled algebraically

$$\tilde{V} = \tilde{I} \cdot (R + j \cdot (X_L - X_C))$$

  - < 5 Hz modulation bandwidth
  - Electromechanical oscillations and some controls modeled dynamically
  - Handles very large systems

Case Studies

Objectives:

- To evaluate DG impact on Grid power quality, protection and stability
- To identify DG design improvements and DG/EPS interconnect interface requirements

Power Quality

- **Voltage Regulation**
- **Flicker**
- Unbalanced grid
- Harmonics
- DC current injection
- Grounding

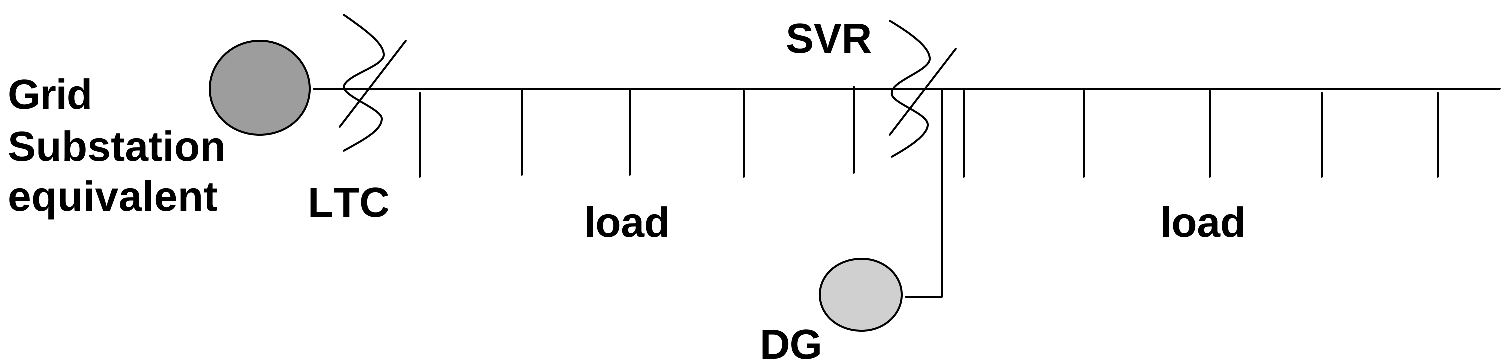
Protection and Stability

- Capacitor switching
- Fault analysis
- **Anti-islanding protection**
- Reclosing
- Stability
  - local system stability
  - **bulk system stability**
  - **microgrid stability**

Voltage Regulation

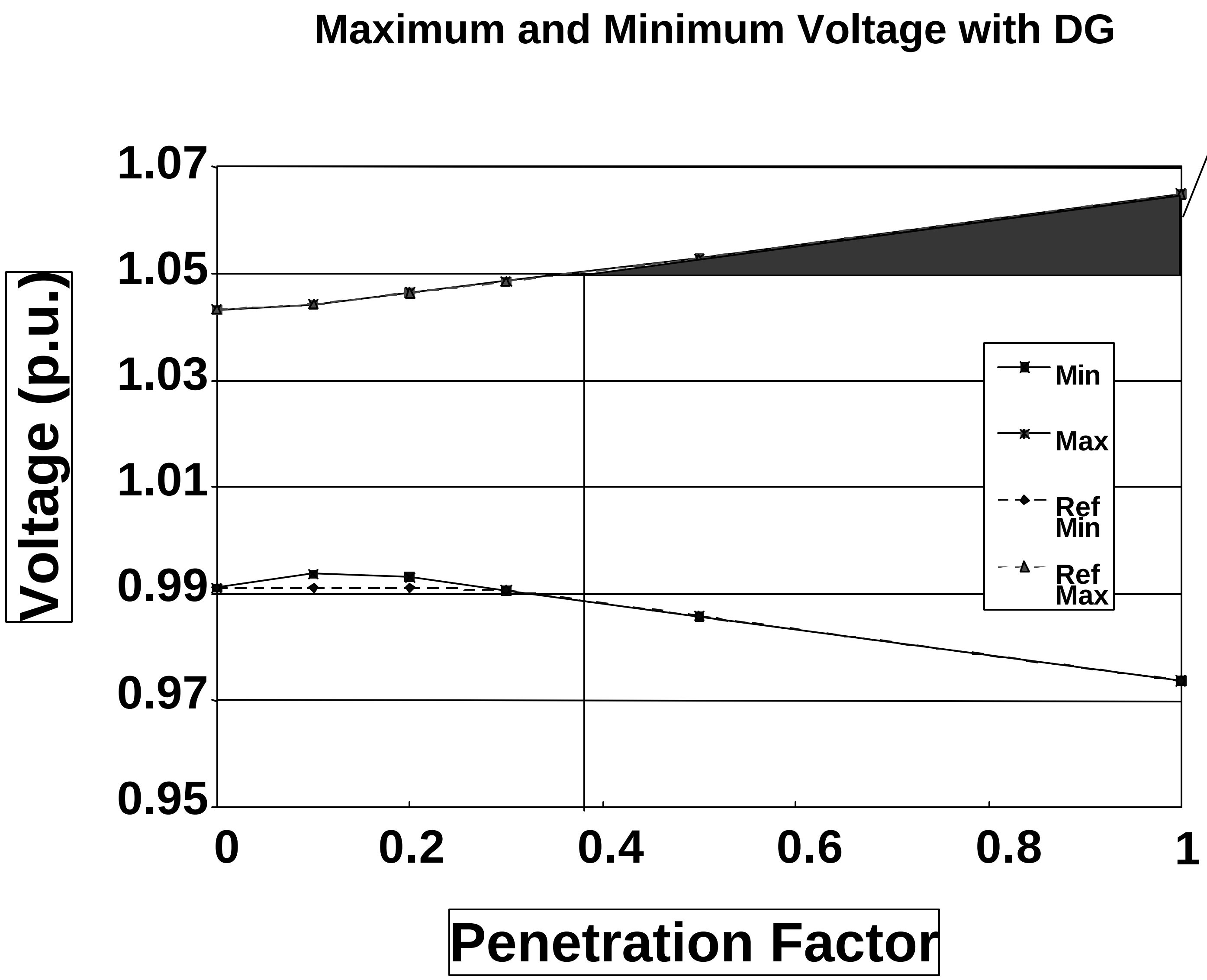
Objectives:
- **Study DG impact on feeder voltage profile**
- **Study DG interaction with LTC and SVR**

Case 1: Generic Radial Feeder Models and Cases for Voltage Regulation Study



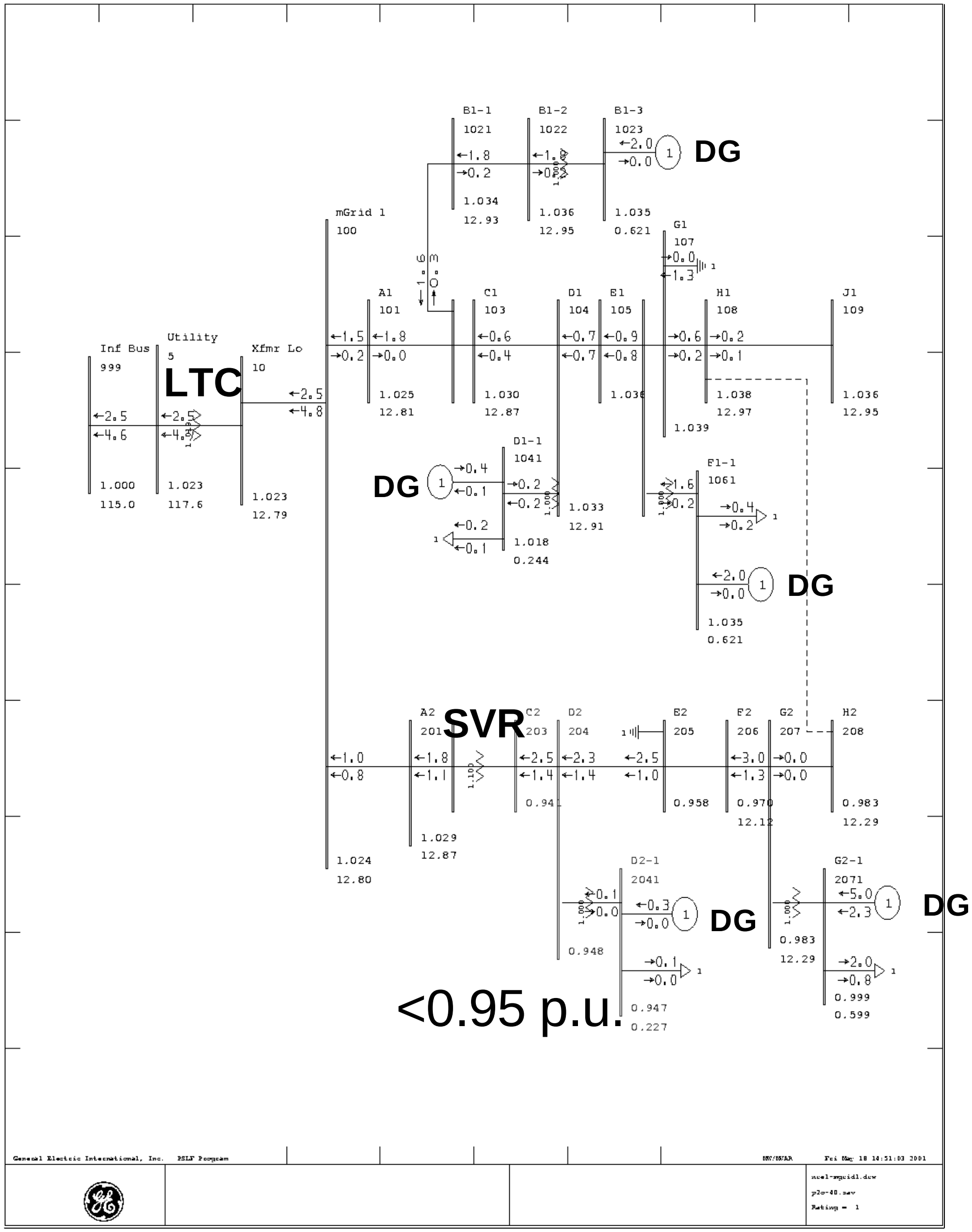
Base Design	Design Variation	Substation LTC Control				CAPACITOR BANKS[1] kVAr Rating*	SVR Control				DG Voltage Regulation[3]
		Voltage Setpoint	Load Drop Compensation Settings				Voltage Setpoint	Load Drop Compensation Settings			
			R (W)	X (W)	Voltage Limit			R (W)	X (W)	Voltage Limit	
Case 1: 4 mile Feeder	**1.1**	1.05	No LDC		Fixed	0	-No SVR-				Secondary
	1.2	1.04	0.30	0.60	1.05	0	No SVR				Secondary
	1.3	1.05	0.00	0.00	1.05	Varied[2]	No SVR				Secondary
Case 2: 8 mile Feeder	**2.1**	1.01	0.75	1.50	No limit	900	No SVR				Secondary
	2.2	1.02	0.60	1.10	1.05	1200	No SVR				Secondary
Case 3: 8 mile Feeder	**3.1**	1.02	0.50	1.00	No limit	900	1.01	1.00	2.00	No limit	Secondary
	3.2	1.03	0.25	0.50	1.05	900	1.03	0.60	1.10	1.05	Secondary
	3.3	1.03	0.25	0.50	1.05	900	1.03	0.60	1.10	1.05	Primary

Global Voltage Profile v.s. DG Penetration



DG can cause high voltages at light load for significant penetrations

Voltage Regulation

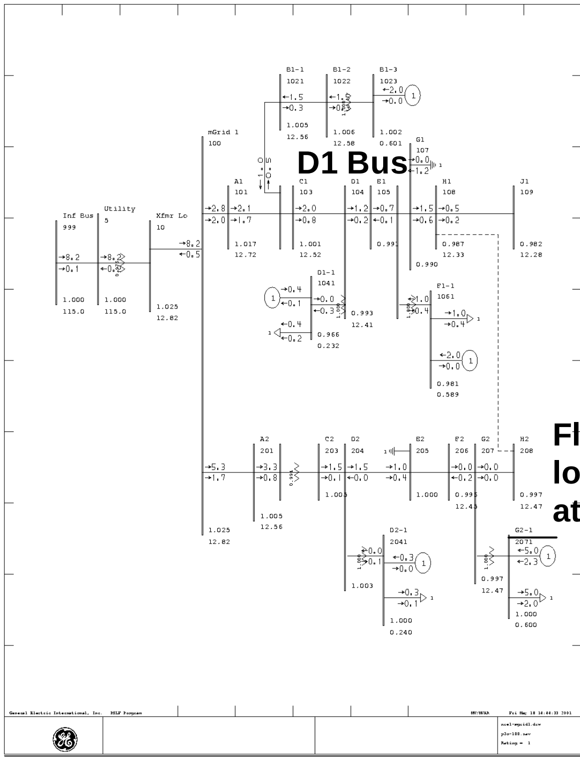


Case 2:
DG interaction with SVR

- SVR adjusts voltage set points based on locally measured real and reactive current flow.
- The presence of DG (5 DGs in this example) causes localized changes in flow patterns
- The interaction may cause unstable SVR regulation and result in out-of-range voltage (0.94 p.u.), as highlighted in the Figure.

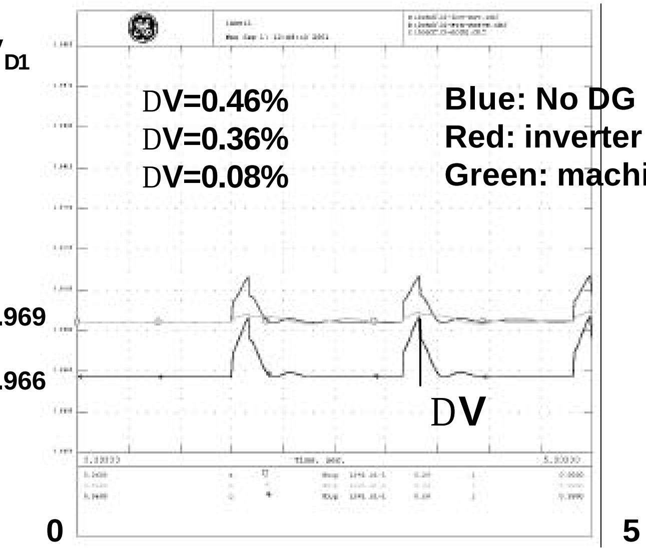
Flicker

Objective: Study DG impact on load induced flicker



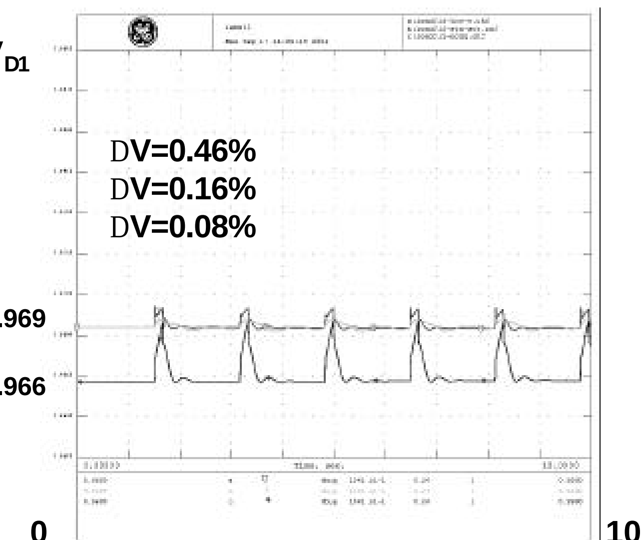
Flicker load pulsations at 0.6Hz

V_{D1}



DG Without voltage regulation

V_{D1}

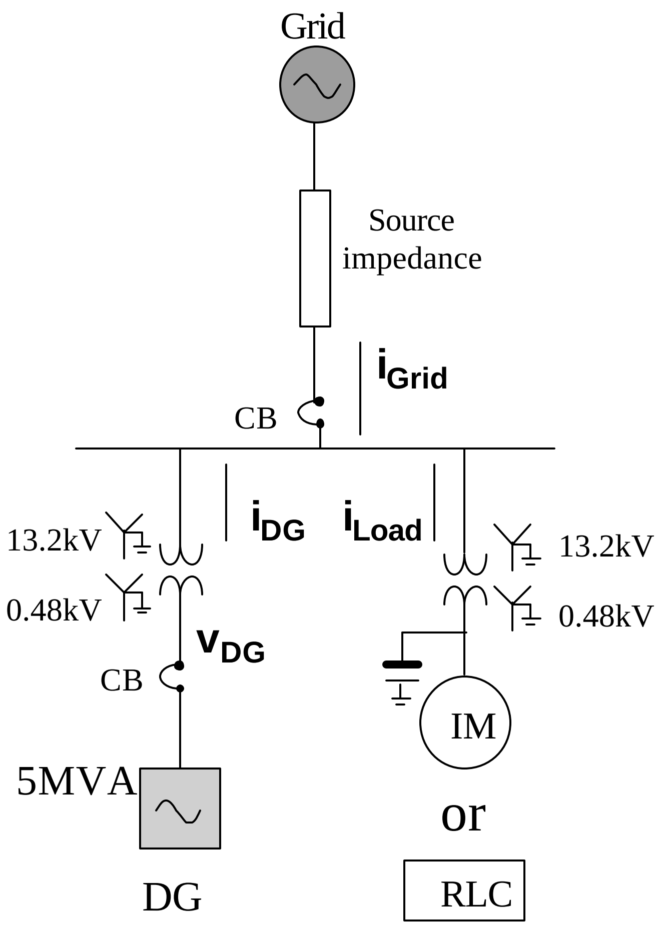


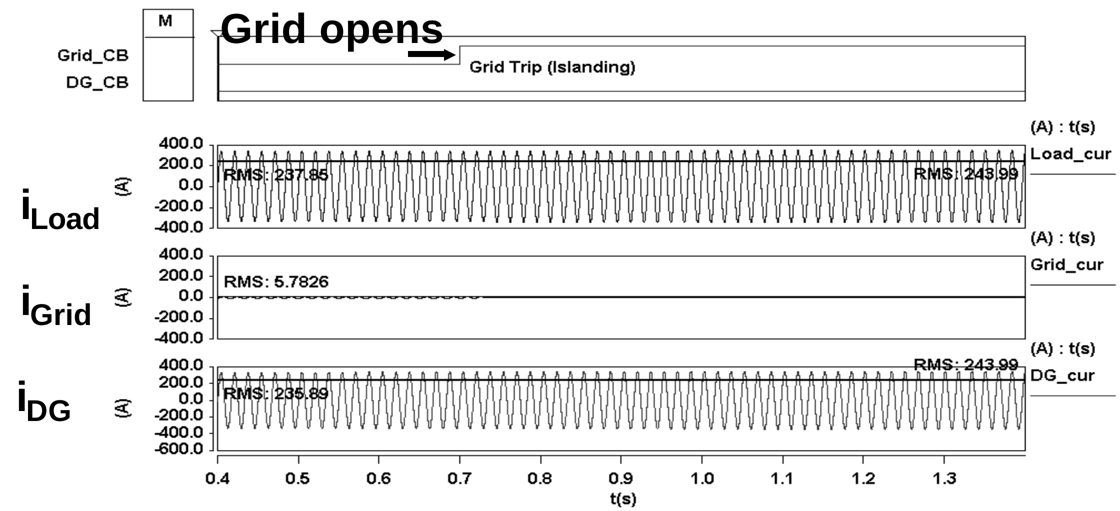
DG with voltage regulation

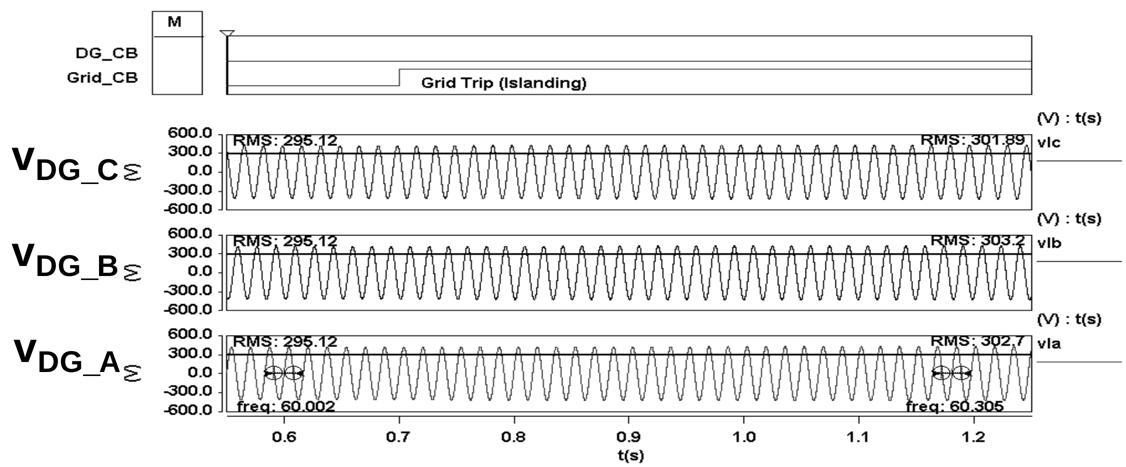
- Inverter DG has a slight beneficial impact on the load induced flicker
- Machine DG has a substantial beneficial impact due to increased short circuit strength
- Inverter DG with voltage regulation has a significant improvement

Anti-Islanding

Objective:
Study worst-case load using Sandia's scheme as an example.





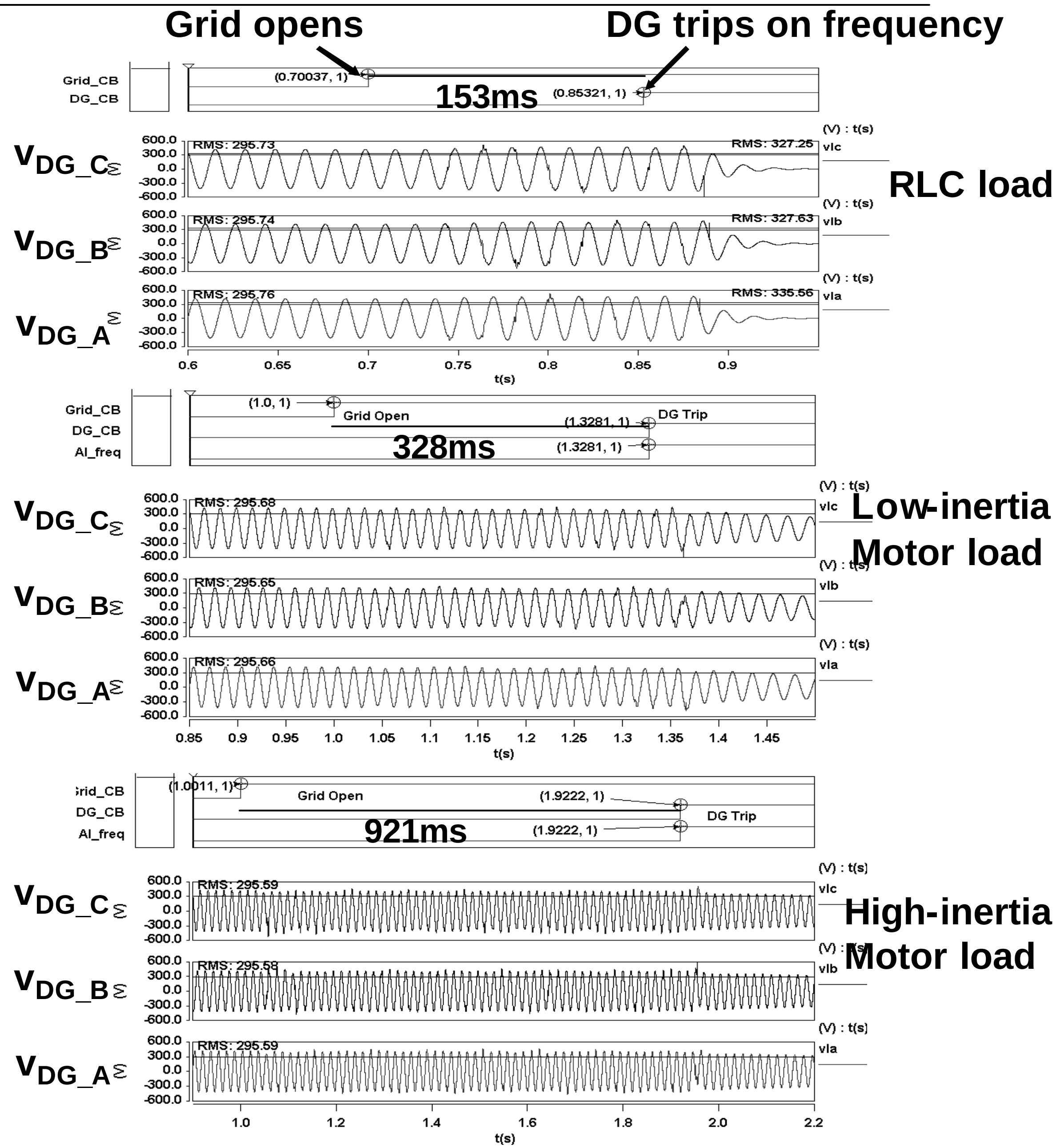


• Without active anti-islanding, it is highly possible that an island may be formed if DG and load are closely matched

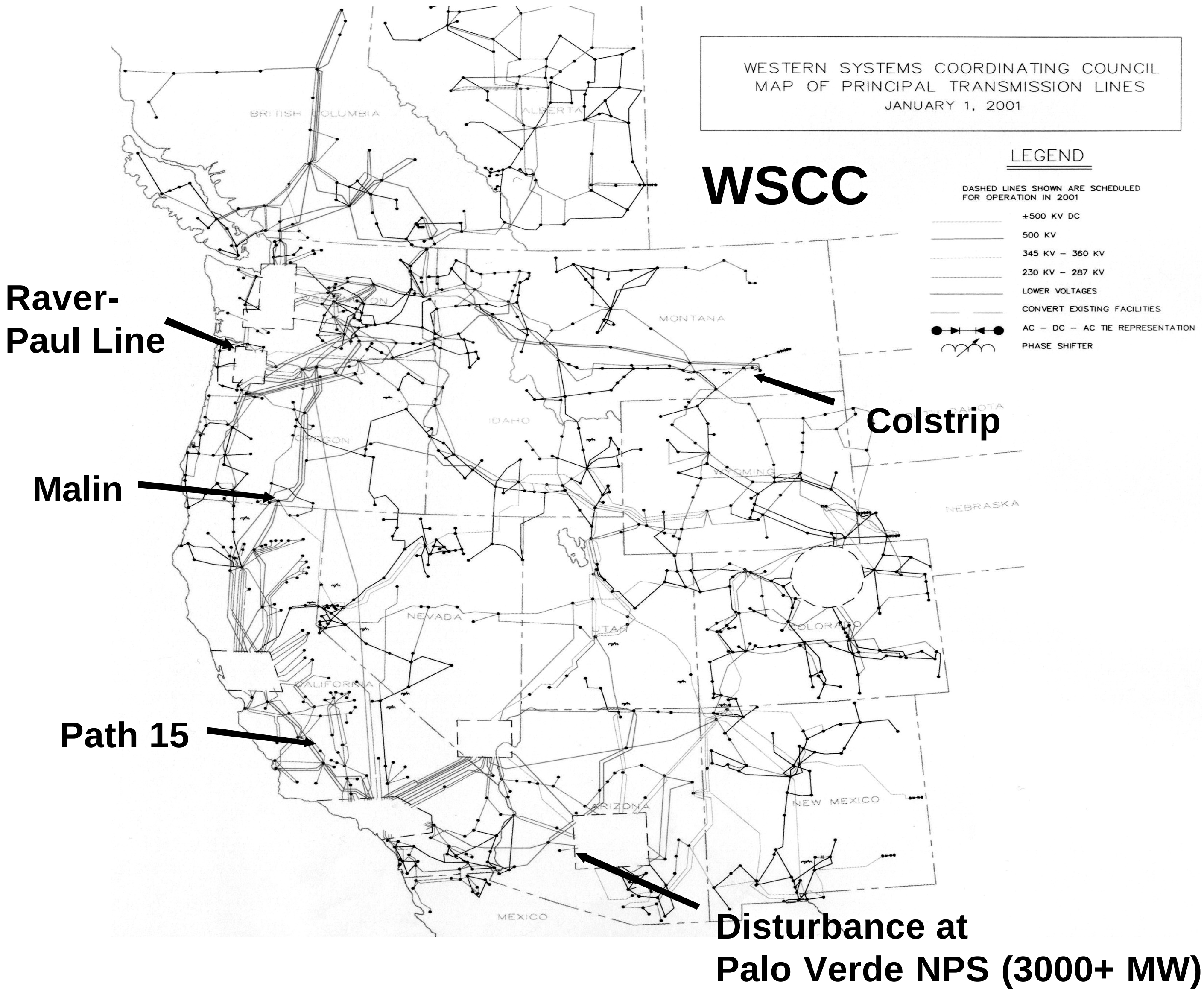
Anti-Islanding with Different Loads

- Active anti-islanding can detect island condition with different loads.

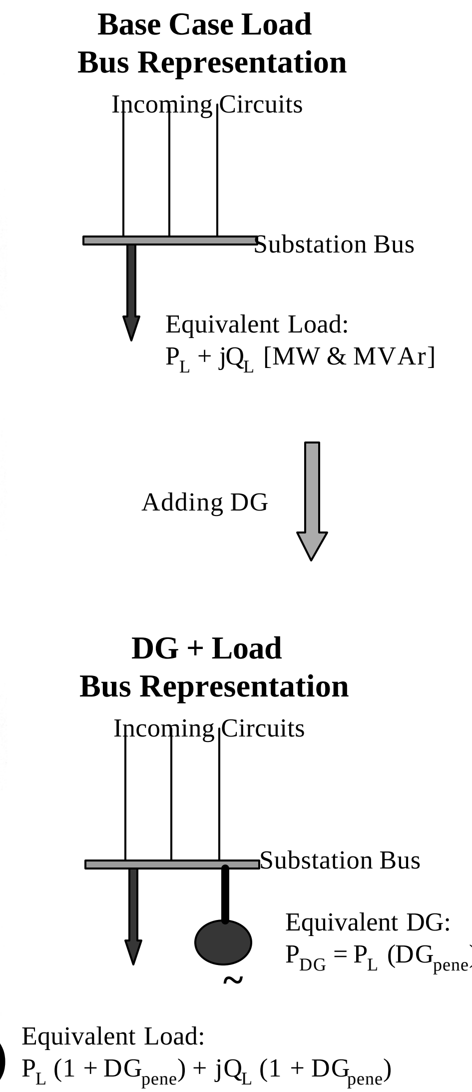
- There is much longer run-on time for high-inertia motor load than RLC load and low-inertia motor load. Therefore, motor load is more challenging for anti-islanding detection.



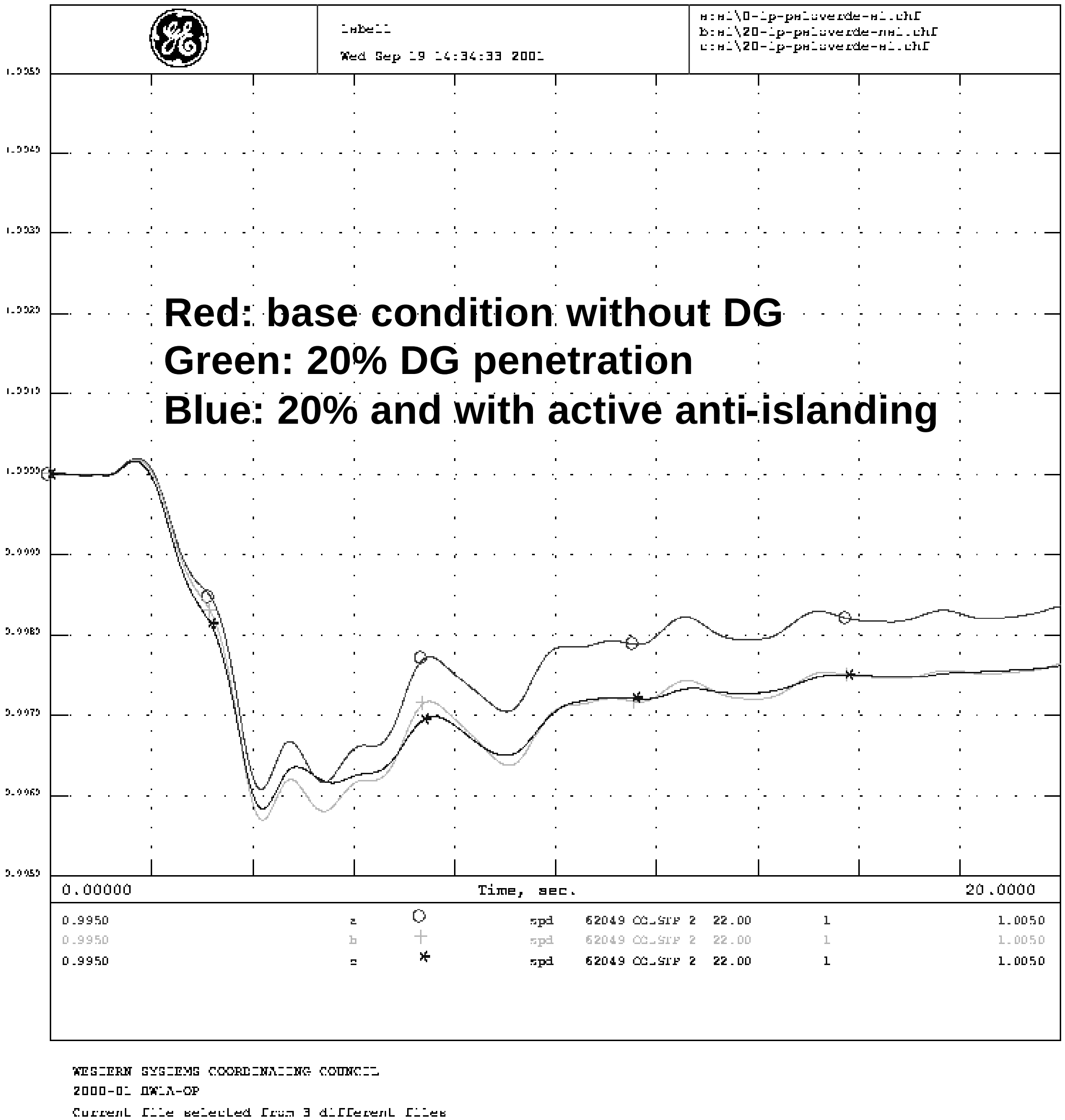
DG Impact on Bulk Power System



>6000 DGs Modeled:



Active Anti-Islanding Impact on Bulk Power System



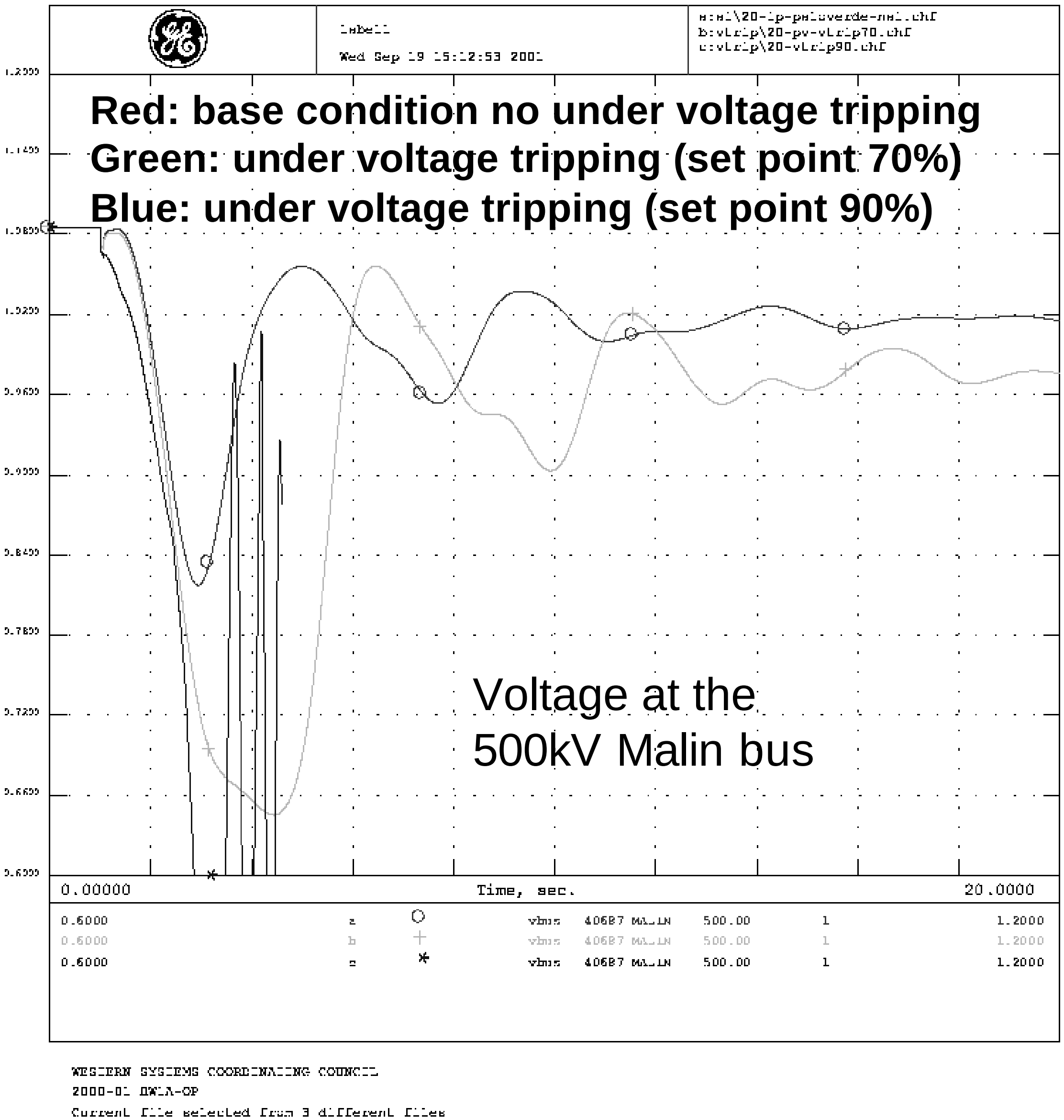
- Disturbance event:
a very large power station with multiple units generating over 3000 MW in WSCC system is assumed to be tripped off-line by some common-mode disturbance.

- The case illustrates that the aggregate impact of the active anti-islanding scheme is benign to the system performance

- The lack of frequency regulation by DGs aggravates the common-mode frequency depression

Bulk System frequency dynamics with high DG Penetration and impact of Anti-islanding

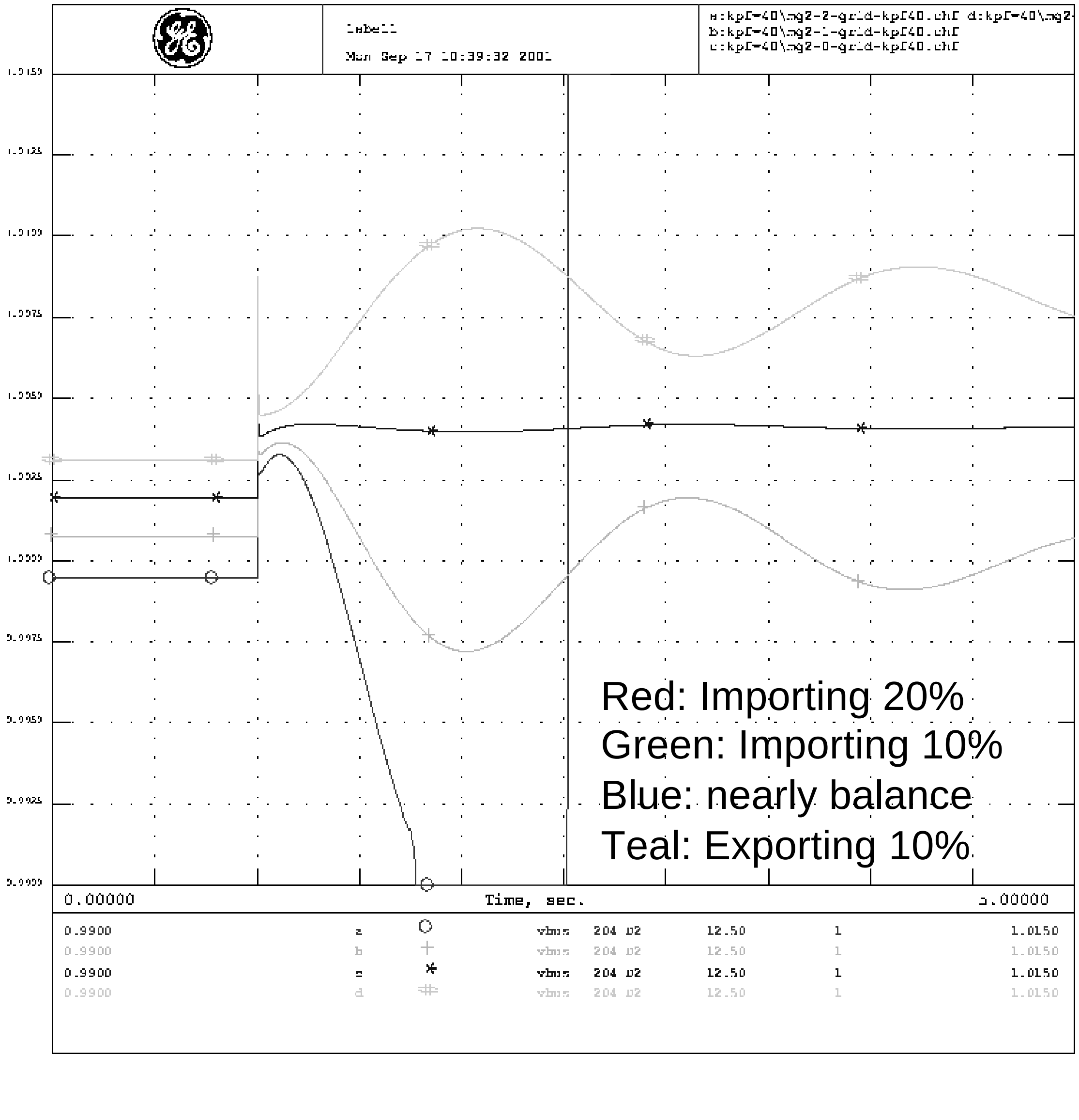
DG Tripping impact on Bulk System Stability



- Most new DGs standards dictate disconnect for voltages <70% for a specified period.
- It is important to note that these documents specify the *minimum* voltage and the *maximum* time to trip. Thus, DGs will be in violation if they trip slower or at too low a voltage. However, the DGs may trip faster and at higher voltages than this without violation.
- The case (blue trace) with the 90% trip point is very unstable

Bulk system voltage dynamics with low voltage DG tripping (20% DG penetration).

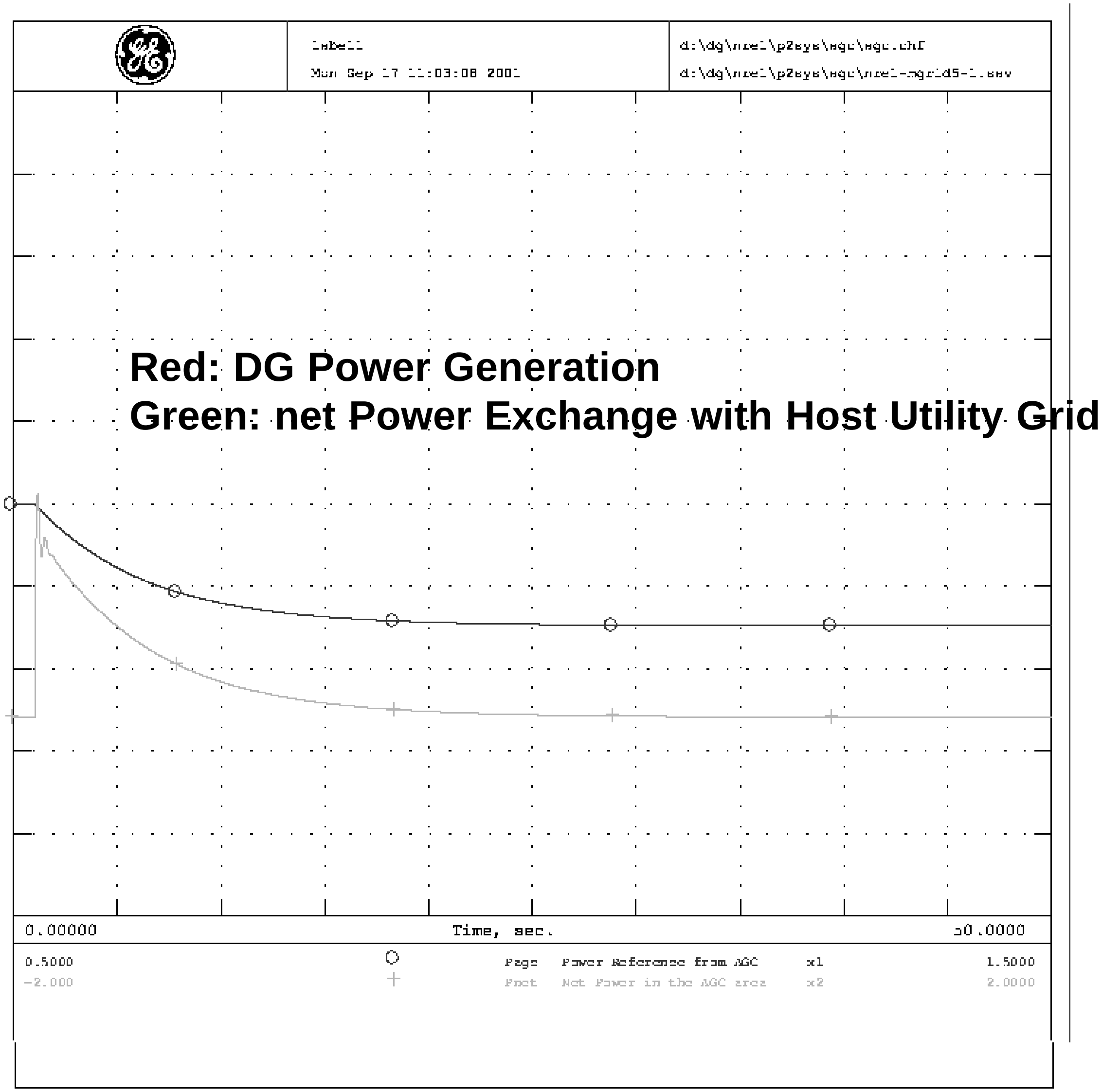
MicroGrid Dynamics



- Microgrid (P2 system) is islanded from the host grid under four different conditions
- DGs have voltage and frequency regulation
- Microgrid can operate stably following disconnection from the grid with autonomous proportional controls, as long as the power export (or import) before the disturbance is not too large.

Microgrid voltage at bus D2 following islanding from bulk system.

MicroGrid with Supervisory Control on Interchange



Response of MicroGrid with Supervisory to a load disruption utility

MicroGrid Control can maintain a scheduled interchange with the host utility

Major Take-aways from Case Studies

- **Power Quality**
  - Modest penetration of DG has relatively little effect on system voltage. High penetrations add challenges for voltage regulation, and may require additional controls/intelligence/communication
  - Inverter-type DGs will have potential significant beneficial impact on flicker caused by system loads
- **Protection and Reliability**
  - Inverter based DG systems act essentially as ideal current sources. Therefore minimal fault current contributions have little effect on overcurrent protection
  - Widespread penetration of DGs at the load appears to be benign with respect to system response to bulk system disturbances
  - DGs designed with overly aggressive trip characteristics pose a system risk
  - Active anti-islanding schemes in distribution systems with multiple DGs and significant motor loads appear to work well
  - Microgrids with DGs can exhibit good performance.

Next Step

TASKS	COMPLETION DATE
• Identify improvements in DG design and requirements for DG-EPS Interface	Dec. 2001
• Conceptual Design for DG-EPS Interface	Dec. 2001
• Contribution to IEEE P1547	Ongoing